

AMENDMENTS TO THE CLAIMS:

1. (Canceled)

2. (Currently amended) An input circuit comprising:

a data input means for ~~the input of~~ receiving input data of the input circuit;

a data latch means for latching ~~the input data~~ output data of the input circuit;

a reset means for resetting the data latch means in response to a first logic level of a first clock signal;

a latch enhancement means for enhancing a latching operation of the data latch means in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal; and

a clock synchronization means for ~~blocking a feedthrough current by functioning complementarily to the reset means and synchronizing the input of the input data to the data input means~~ transferring the input data from the data input means to the data latch means in response to a second logic level of the first clock signal.

the clock synchronization means blocking a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first and second clock signals are in a first logic level state; and

~~a latch enhancement means for enhancing the latching operation of the data latch means.~~

3. (Currently amended) An input circuit comprising:

a data input means for ~~the input of~~ receiving input data of the input circuit;

a data latch means ~~that provides a combined function of blocking feedthrough current in the reset state and synchronizing the latch of the input data connected to the data input means and including an activating means for activating the data latch means and inputting the input data in response to a first logic level of a first clock signal~~;

a reset means for resetting the data latch means in response to a second logic level of the first clock signal; and

a latch enhancement means for enhancing ~~the~~ a latching operation of the data latch means in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal.

wherein said activating means blocks a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first clock signal is in a second logic level state and the second clock signal is in a first logic level state.

4.-9. (Canceled)

10. (Currently amended) The input circuit of claim 2, wherein:

the data input means ~~includes the~~ comprises sources of both a ~~tenth~~ first NMOS transistor and an ~~eleventh~~ a second NMOS transistor being connected to ~~the second~~ a power source via said clock synchronization means;

the a gate of the ~~tenth~~ first NMOS transistor being connected to a first data input terminal;

the a gate of the ~~eleventh~~ second NMOS transistor being connected to a second data input terminal;

the a drain of the ~~tenth~~ first NMOS transistor being connected to a ~~third~~ common terminal at which one of a pair of complementary signals constituting the input data appears; and

the a drain of the ~~eleventh~~ second NMOS transistor being connected to a ~~fourth~~ common terminal at which ~~the other~~ another one of the pair of complementary signals constituting the input data appears.

11. (Currently amended) The input circuit of claim 2, wherein the clock synchronization means ~~includes the~~ comprises gates of ~~twelfth~~ a first NMOS transistor and ~~thirteenth~~ a second NMOS transistor being connected to ~~the~~ a first clock input terminal; ~~the~~ a source of the ~~twelfth~~ first NMOS transistor being connected, via said data input means, to a ~~third~~ common terminal at which one of a pair of complementary signals constituting the input data appears; ~~the~~ a source of the ~~thirteenth~~ second NMOS transistor being connected, via said data input means, to a ~~fourth~~ common terminal at which the other one of the pair of complementary signals constituting the input data appears; ~~the~~ a drain of the ~~twelfth~~ first NMOS transistor being connected to a ~~first~~ common terminal; and ~~the~~ a drain of the ~~thirteenth~~ second NMOS transistor being connected to a ~~second~~ common terminal.

12. (Currently amended) The input circuit of claim 2, wherein:

the latch enhancement means ~~includes~~ comprises the sources of both a ~~fourteenth~~ first NMOS transistor and a ~~fifteenth~~ second NMOS transistor being connected to a ~~second~~ power source via said clock synchronization means;

~~the~~ gates of both the ~~fourteenth~~ first NMOS transistor and the ~~fifteenth~~ second NMOS transistor being connected to a ~~second~~ clock input terminal;

~~the~~ a drain of the ~~fourteenth~~ first NMOS transistor being connected to a ~~third~~ common terminal at which one of a pair of complementary signals constituting the input data appears; and

~~the~~ a drain of the ~~fifteenth~~ second NMOS transistor being connected to a ~~fourth~~ common terminal at which ~~the other~~ another one of the pair of complementary signals constituting the input data appears.

13-17. (Canceled)

18. (New) An input circuit comprising:

a data input unit that receives input data of the input circuit;

a data latch unit that latches output data of the input circuit;

a reset unit that resets the data latch unit in response to a first logic level of a first clock signal;

a latch enhancement unit that enhances a latching operation of the data latch unit in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal; and

a clock synchronization unit that transfers the input data from the input unit to the data latch unit in response to a second logic level of the first clock signal,

the clock synchronization unit blocking a feedthrough current that flows through the reset unit, the data latch unit, and the latch enhancement unit when the first and second clock signals are in a first logic level state.

19. (New) An input circuit comprising:

a data input unit that receives input data of the input circuit;

a data latch unit, connected to the data input unit, that latches output data of the input circuit, the data latch unit having an activating unit that activates the data latch unit and inputs the input data in response to a first logic level of a first clock signal;

a reset unit that resets the data latch unit in response to a second logic level of the first clock signal;

a latch enhancement unit that enhances a latching operation of the data latch unit in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal,

wherein said activating unit blocks a feedthrough current that flows through the reset unit, the data latch unit, and the latch enhancement unit when the first clock signal is in a second logic level state and the second clock signal is in a first logic level state.